



PATENT
Attorney Docket No. 211467-00211

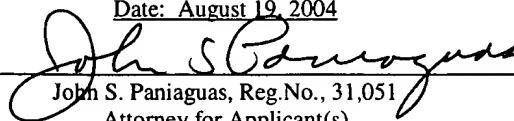
IN THE U.S. PATENT AND TRADEMARK OFFICE

Application No.: 09/833,372)
Filing Date: April 12, 2001)
Inventor(s): Michael Wojtowicz)
Group Art Unit: 2815)
Examiner Name: Baumeister, Bradley W.)
Customer No.: 27160)
Title: GaN HBT SUPERLATTICE BASE)
STRUCTURE)

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Office, with sufficient postage, via first class mail to Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: August 19, 2004


John S. Paniaguas, Reg. No., 31,051
Attorney for Applicant(s)

Mail Stop Non-Fee Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT TRANSMITTAL

Sir:

Transmitted herewith is an amendment/reply in the above-identified application.

1. () A paper requesting correction/substitution of drawings is attached.
2. Fee for Claims

No additional fee is required.

The fee for additional claims in accordance with 37 C.F.R. §1.16(b)-(d) has been calculated as shown below:

				SMALL ENTITY		OTHER THAN A SMALL ENTITY	
	Claims Remaining After Amendment	Highest No. Previously Paid for	Present Extra	Rate	Additional Fee	Rate	Additional Fee
Total	2	Minus	20	0	x 9	0	x 18
Indep.	2	Minus	3	0	X 43	0	x 86
Fee for Multiple Dependent Claims				+145	0	+290	--
TOTAL ADDITIONAL FEES				0	OR	<hr/>	

3. **Method of Payment of Fees**

() Enclosed is our firm check in the amount of: \$

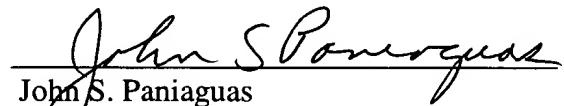
() Charge \$_____ to Deposit Account No. 50-1214.

4. (X) The Commissioner is hereby authorized to charge any additional fees which may be required in this application under 37 C.F.R. §§1.16-1.17 during its entire pendency, or credit any overpayment, to Deposit Account No. 50-1214. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 50-1214. This sheet is filed in duplicate.

Respectfully Submitted,

August 19, 2004
(Date)

By:


John S. Paniaguas
Registration No. 31,051

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IFW 2815

PATENT
ATTORNEY DOCKET NO. 211467-00211

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Michael Wojtowicz

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) P.O. Box 1450
) Alexandria, VA22313-1450
) *8/19/4 John S. Paniaguas*
) Date *John S. Paniaguas*
) Registration No.31,051

Application No.: 09/833,372

Filed: April 12, 2001

Title: GaN HBT SUPERLATTICE BASE
STRUCTURE

Group Art Unit: 2815

Examiner: Baumeister, Bradley W.

Mail Stop Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Official Action mailed on March 19, 2004, please enter the following amendment.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

a substrate formed from a material selected from the group consisting of sapphire and silicon carbide;

an n+ doped GaN subcollector layer;

an n- doped GaN collector layer;

a p+ doped base layer formed on top of said collector layer defining a base collector interface formed from alternating layers of AlGaN/GaN forming a superlattice;

an n+ doped AlGaN emitter layer formed on top of said base layer defining an emitter base interface;

a base contact formed on said base layer;

a collector contact formed on said subcollector; and

an emitter contact formed on said emitter.

6. (Canceled).

7. (Canceled).

8. (Original). A method for fabricating a heterojunction bipolar transistor comprising the steps:

(a) forming a subcollector layer on a substrate;

(b) forming a collector layer on said collector layer;

(c) forming a base layer as a superlattice of alternating layers of AlGaN/GaN on said collector defining a base collector interface; said base layer formed with an irregular band gap energy;

(d) forming an emitter layer on said base layer defining a base collector interface; and

(e) forming contacts on said base, subcollector said emitter layers.

9. (Original). A method for fabricating a heterojunction bipolar transistor comprising the steps:

(a) forming a subcollector layer on said substrate;

(b) forming a collector layer on said subcollector layer;

(c) forming a base layer comprising a superlattice of alternating layers of AlGaN/GaN having a non-constant concentration of Al in said alternating layers of